## 74AHC3G04; 74AHCT3G04

Inverter

Rev. 4 — 19 November 2018

### 1. General description

The 74AHC3G04; 74AHCT3G04 are high-speed Si-gate CMOS devices. They provide three inverting buffers.

The AHC device has CMOS input switching levels and supply voltage range 2 V to 5.5 V.

The AHCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

### 2. Features and benefits

- Symmetrical output impedance
- High noise immunity
- ESD protection:
  - HBM JESD22-A114F exceeds 2 000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101C exceeds 1 000 V
- Low power dissipation
- Balanced propagation delays
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

### 3. Ordering information

#### Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC3G04DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74AHC3G04DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package;	SOT765-1
74AHCT3G04DC	_		8 leads; body width 2.3 mm	

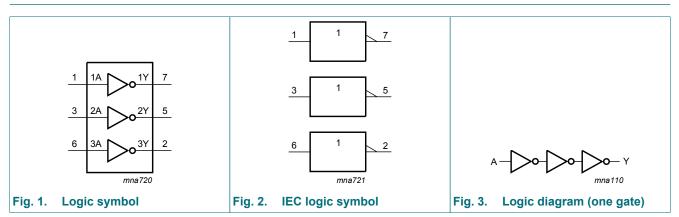
### 4. Marking

Table 2. Marking codes					
Type number	Marking code[1]				
74AHC3G04DP	A04				
74AHC3G04DC	A04				
74AHCT3G04DC	C04				

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

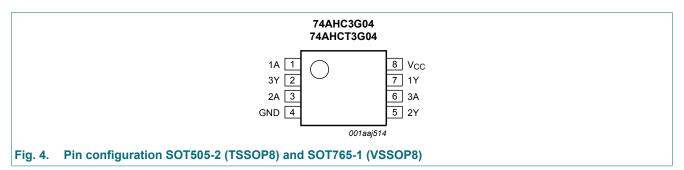
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### 5. Functional diagram



### 6. Pinning information

#### 6.1. Pinning



### 6.2. Pin description

#### Table 3. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 6	data input
GND	4	ground (0 V)
1Y, 2Y, 3Y	7, 5, 2	data output
V <sub>CC</sub>	8	supply voltage

### 7. Functional description

#### Table 4. Function table

*H* = *HIGH* voltage level; *L* = *LOW* voltage level

Input nA	Output nY
L	Н
Н	L

### 8. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+7.0	V
VI	input voltage			-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V	[1]	-20	-	mA
I <sub>ОК</sub>	output clamping current	$V_{\rm O}$ < -0.5 V or $V_{\rm O}$ > $V_{\rm CC}$ + 0.5 V	[1]	-	±20	mA
I <sub>O</sub>	output current	$-0.5 V < V_O < V_{CC} + 0.5 V$		-	±25	mA
I <sub>CC</sub>	supply current			-	75	mA
I <sub>GND</sub>	ground current			-75	-	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P<sub>tot</sub> derates linearly with 2.5 mW/K.

For VSSOP8 package: above 110 °C the value of Ptot derates linearly with 8 mW/K.

### 9. Recommended operating conditions

#### Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74	4AHC3G	04	74	Unit		
			Min	Тур	Max	Min	Тур	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
VI	input voltage		0	-	5.5	0	-	5.5	V
Vo	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and	$V_{CC}$ = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V
	fall rate	$V_{CC}$ = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V

### **10. Static characteristics**

#### Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Тур	Мах	Min	Max	Min	Max	
74AHC3	G04									
VIH	HIGH-level	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
	input voltage	V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V <sub>IL</sub>	LOW-level	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
	input voltage	V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V

Symbol	Parameter	Conditions		25 °C		-40 °C	to +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Мах	Min	Max	Min	Мах	1
V <sub>OH</sub>	HIGH-level	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
	output voltage	I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		$I_{\rm O}$ = -8.0 mA; $V_{\rm CC}$ = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level	$V_{I} = V_{IH} \text{ or } V_{IL}$								
	output voltage	I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
l <sub>l</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	1.0	-	10	-	40	μA
CI	input capacitance		-	1.5	10	-	10	-	10	pF
74AHCT	3G04					1		I	I	-
V <sub>IH</sub>	HIGH-level input voltage	$V_{CC}$ = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level	$V_{I}$ = $V_{IH}$ or $V_{IL}$ ; $V_{CC}$ = 4.5 V								
	output voltage	Ι <sub>Ο</sub> = -50 μΑ	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level	$V_{I} = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
	output voltage	I <sub>O</sub> = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
l <sub>l</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	1.0	-	10	-	40	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = 3.4 V; other inputs at V <sub>CC</sub> or GND; $I_O = 0 A$ ; V <sub>CC</sub> = 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
CI	input capacitance		-	1.5	10	-	10	-	10	pF

### **11. Dynamic characteristics**

#### Table 8. Dynamic characteristics

GND = 0 V; for test circuit see Fig. 6.

Symbol	Parameter	Conditions			25 °C		-40 °C	to +85 °C	-40 °C to +125 °C		Unit
				Min	Тур	Max	Min	Max	Min	Max	
74AHC3	G04								1		-
t <sub>pd</sub>	propagation	nA to nY; see Fig. 5	[1]								
	delay	V <sub>CC</sub> = 3.0 V to 3.6 V	[2]								
		C <sub>L</sub> = 15 pF		-	4.3	7.1	1.0	8.5	1.0	11.0	ns
		C <sub>L</sub> = 50 pF		-	6.1	10.6	1.0	12.0	1.0	14.5	ns
		$V_{CC}$ = 4.5 V to 5.5 V	[3]								
		C <sub>L</sub> = 15 pF		-	3.1	5.5	1.0	6.5	1.0	7.0	ns
		C <sub>L</sub> = 50 pF		-	4.5	7.5	1.0	8.5	1.0	9.5	ns
C <sub>PD</sub>	power dissipation capacitance	per buffer; $C_L = 50 \text{ pF}$ ; $f_i = 1 \text{ MHz}$ ; $V_I = \text{GND to } V_{CC}$	[4]	-	9	-	-	-	-	-	pF
74AHCT	3G04	1									
t <sub>pd</sub>	propagation delay	nA to nY; See <u>Fig. 5;</u> V <sub>CC</sub> = 4.5 V to 5.5 V	[1][3]								
		C <sub>L</sub> = 15 pF		-	3.4	6.7	1.0	7.5	1.0	8.5	ns
		C <sub>L</sub> = 50 pF		-	4.9	7.7	1.0	8.5	1.0	10.0	ns
C <sub>PD</sub>	power dissipation capacitance	per buffer; $C_L$ = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub>	[4]	-	10	-	-	-	-	-	pF

[1]

 $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}.$  Typical values are measured at V\_{CC} = 3.3 V. Typical values are measured at V\_{CC} = 5.0 V. [2] [3]

[4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

 $P_{D} = C_{PD} \times V_{CC}^{2} \times f_{i} \times N + \Sigma(C_{L} \times V_{CC}^{2} \times f_{o}) \text{ where:}$ 

 $f_i$  = input frequency in MHz;

fo = output frequency in MHz;

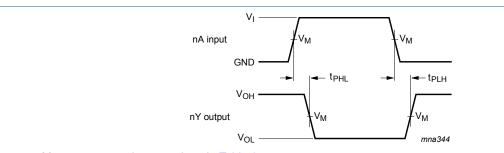
 $C_L$  = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_0)$  = sum of the outputs.

### 11.1. Waveforms and test circuit



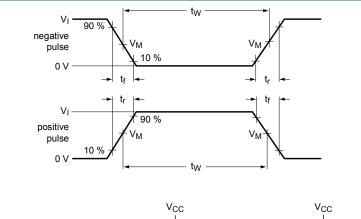
Measurement points are given in <u>Table 9</u>.

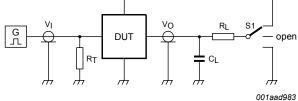
Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

#### Fig. 5. The input (nA) to output (nY) propagation delays

#### Table 9. Measurement points

Туре	Input	Output
	V <sub>M</sub>	V <sub>M</sub>
74AHC3G04	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>
74AHCT3G04	1.5 V	0.5V <sub>CC</sub>





Test data is given in <u>Table 10</u>.

Definitions test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

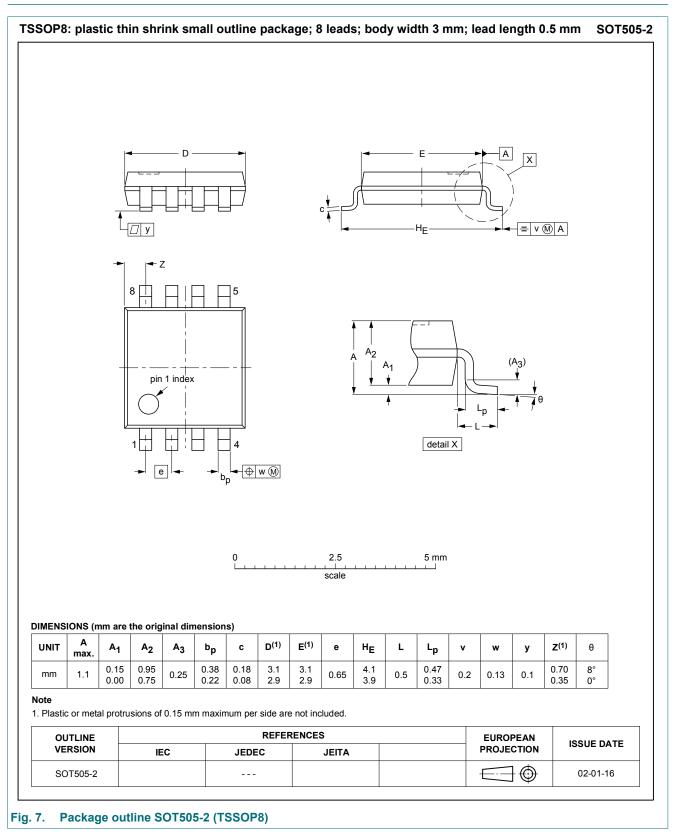
C<sub>L</sub> = Load capacitance including jig and probe capacitance; R<sub>L</sub> = Load resistance; S1 = Test selection switch.

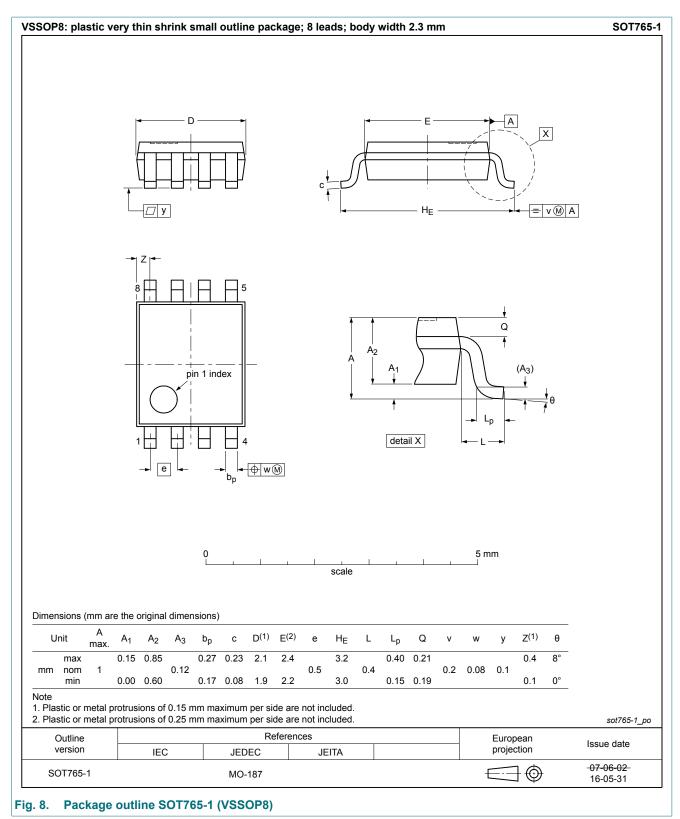
#### Fig. 6. Test circuit for measuring switching times

#### Table 10. Test data

Туре	Input		Load		S1 position		
	VI	t <sub>r</sub> , t <sub>f</sub>	CL	RL	t <sub>PHL</sub> , t <sub>PLH</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>
74AHC3G04	V <sub>CC</sub>	≤ 3 ns	15 pF, 50 pF	1 kΩ	open	GND	V <sub>CC</sub>
74AHCT3G04	3 V	≤ 3 ns	15 pF, 50 pF	1 kΩ	open	GND	V <sub>CC</sub>

### 12. Package outline





### 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

### 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74AHC_AHCT3G04 v.4	20181119	Product data sheet	-	74AHC_AHCT3G04 v.3	
Modifications:	• Type numbers 74AHCT3G04DP, 74AHCT3G04GD and 74AHC3G04GD removed.				
74AHC_AHCT3G04 v.3	20130326	Product data sheet	-	74AHC_AHCT3G04 v.2	
Modifications:	<ul> <li>For type numbers 74AHC3G04GD and 74AHCT3G04GD, XSON8U has changed to XSON8.</li> </ul>				
74AHC_AHCT3G04 v.2	20090126	Product data sheet	-	74AHC_AHCT3G04 v.1	
74AHC_AHCT3G04 v.1	20031106	Product specification	-	-	

74AHC\_AHCT3G04

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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