NISSHINBO

R5542Z Series

6 A Low ON Resistance Nch Load Switch IC with Voltage Detector

NO.EA-335-181030

OUTLINE

The R5542Z is a Nch. load switch IC with a voltage detector. The R5542Z is an ideal load switch IC for supplying the power from the battery to the load circuit. A built-in Nch. driver transistor with typically 9 mΩ ON resistance allows the R5542Z to provide a low dropout voltage and prevents the reverse current during shutdown mode. Internally, the R5542Z consists of an internal voltage step-up circuit, a soft-start circuit, a chip enable circuit and a UVLO circuit.
The R5542Z is offered in an ultra-small WLCSP-12-P3 package which can achieve the smallest possible footprint solution on boards where area is limited.

FEATURES

Load Switch Section

- Input Voltage Range ········ 2.3 V to 5.5 V
- Output Current ········ DC Max. 6 A
- Output Pulsed Current ········ Max. 12 A (Pulsed at 1 ms, 10% Duty Cyce)
- Switch ON Resistance ········ 9 mΩ (V_{IN} = 3.0 V, I_{OUT} = 300 mA)
- Reverse Current Blocking (RCB) during shutdown mode
- Soft-start Function

Voltage Detector Section

- Supply Current ········ Typ. 1.0 µA (V_{VDI} = 2.0 V)
- Operating Voltage Range ········ 1.2 V to 5.5 V (Ta = 25°C)
- Detector Threshold Range ········ 2.0 V to 5.0 V (0.1 V steps)
- Detector Threshold Accuracy ········ ±2.0%
- Detector Threshold Temperature Coefficient ········ Typ. ±100 ppm/°C
- Output Type ········ CMOS
- Package ········ WLCSP-12-P3

APPLICATIONS

- Smart Phones, Tablet PCs
- Storage, Portable Devices

SELECTION GUIDE

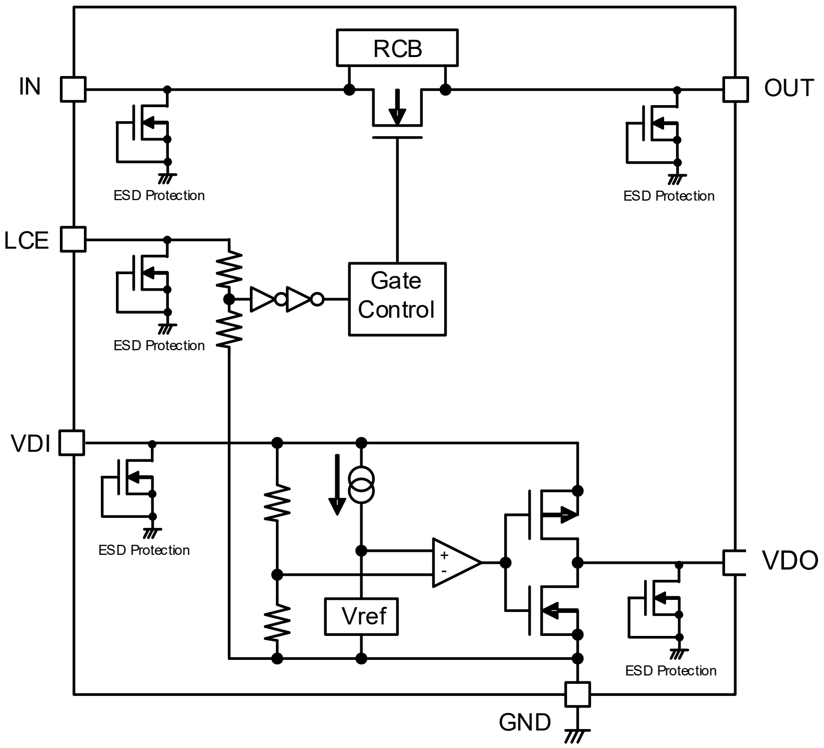
The detector threshold is a user-selectable option.

Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5542Zxx2B-E2-F	WLCSP-12-P3	4,000 pcs	Yes	Yes

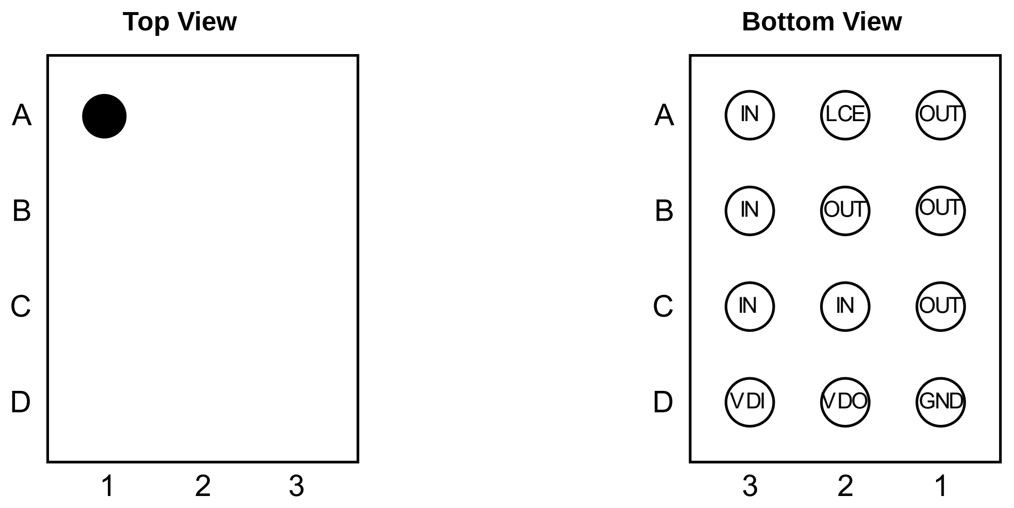
xx: Specify the detector threshold within the range of 2.0 V (20) to 5.0 V (50) in 0.1 V steps.

BLOCK DIAGRAMS



R5542Zxx2B Block Diagram

PIN DESCRIPTIONS



R5542Z (WLCSP-12-P3) Pin Configurations

R5542Z Pin Descriptions

Pin No.	Symbol	Pin Description
A1, B1, B2, C1	OUT	Load Switch Output Pin
A3, B3, C2, C3	IN	Load Switch Input Pin
A2	LCE	Load Switch Control Enable Pin
D1	GND	Ground Pin
D2	VDO	Voltage Detector Output Pin
D3	VDI	Voltage Detector Input Pin

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings

Symbol	Item	Rating	Unit
V_{IN}	Load Switch Input Voltage	−0.3 to 6.0	V
V_{OUT}	Load Switch Output Voltage	−0.3 to V_{IN} + 0.3	V
V_{LCE}	L_{CE} Pin Voltage	−0.3 to 6.0	V
V_{VDI}	VDI Pin Voltage	−0.3 to 6.0	V
V_{VDO}	VDO Pin Voltage	−0.3 to V_{VDI} +0.3	V
V_{PP}	Pin to Pin Voltage	−0.3 to 6.0	V
I_{OUT}	Load Switch Output Current	6.0	A
I_{PULSE}	Load Switch Output Pulsed Current (Pulsed at 1ms, 10% Duty Cycle)	12.0	A
P_D	Power Dissipation(1) (WLCSP-12-P3, JEDEC STD.51-9)	1000	mW
Tj	Junction Temperature Range	−40 to 125	°C
Tstg	Storage Temperature Range	−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS
Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	2.3 to 5.5	V
Ta	Operating Temperature Range	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS
All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

(1) Refer to *POWER DISSIPATION* in *SUPPLEMENTSRY ITEMS* for detail information.

ELECTRICAL CHARACTERISTICS

V_{IN} = 2.3 V to 5.5 V, I_{OUT} = 1 mA, C_{IN} = 1 µ**F,** C_{OUT} = None, unless otherwise noted.
The specifications surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

Electrical Characteristics (Ta = 25°C)

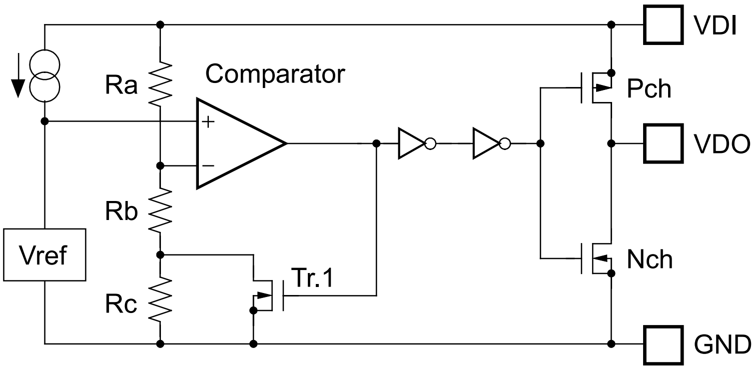
Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
Load Switch Section						
I_Q	Quiescent Current	I_{OUT} = 0 mA		10	30	µA
$I_{Q(OFF)}$	Standby Current	V_{LCE} = 0 V, V_{IN} = 5.5 V, V_{OUT} =OPEN			1	µA
I_{SD}	Shutdown Current	V_{LCE} = 0 V, V_{IN}= 5.5 V, V_{OUT} =GND			1	µA
Ron	Switch ON Resistance	I_{OUT} = 300 mA, V_{IN} = 3 V		9		mΩ
V_{IH}	LCE Pin Input Voltage, high	V_{IN} = 5.0 V	1.0			V
V_{IL}	LCE Pin Input Voltage, low	V_{IN} = 5.0 V			0.4	V
R_{LCE_PD}	LCE Pull-down Resistance	V_{IN} = 2.3 V to 5.5 V		5.5		MΩ
I_{LCE}	LCE Input Leakage Current	V_{IN} = 2.3 V to 5.5 V, V_{LCE} = GND	−1		1	µA
ton	Turn-on Time	V_{IN} = 3 V, R_L = 50 Ω, C_{OUT} = 10 µF		2		ms
UVLO	Undervoltage Lockout Voltage(1)		2.0		2.3	V
Voltage Detector Section						
$-V_{DET}$	Detector Threshold(2)	V_{VDI} falling	$-V_{SET}$ x 0.98		$-V_{SET}$ x 1.02	V
V_{HYS}	Detector Threshold Hysteresis		$-V_{SET}$ x0.03	$-V_{SET}$ x0.05	$-V_{SET}$ x0.07	V
I_{SS}	Supply Current	2.0V < $-V_{SET}$, V_{VDI} = 2.0V		1.0		µA
		2.0V ≤ $-V_{SET}$ ≤ 5.0V, V_{VDI} = $-V_{SET}$ −0.16V			3.3	µA
		2.0V ≤ $-V_{SET}$ ≤ 5.0V, V_{VDI} = $-V_{SET}$ +0.50V			3.4	µA
V_{VDI}	Voltage Detector Operating Voltage	Ta = 25°C	1.2(3)		5.5	V
		−40°C ≤ Ta ≤ 85°C	1.3(3)		5.5	V
I_{VDO}	Output Current (Nch. Driver Output Pin)	2.0 ≤ $-V_{SET}$ ≤ 5.0 V, V_{DS} = 0.5 V, V_{VDI} = 1.5 V	1.0	2.0		mA
	Output Current (Pch. Driver Output Pin)	2.0 ≤ $-V_{SET}$ ≤ 5.0 V, V_{DS} = −2.1 V, V_{VDI} = 5.5 V,	1.0	2.5		mA
t_{PLH}	Release Output Delay Time(4)				100	µs
$\Delta -V_{DET}$ /ΔTa	Detector Threshold Temperature Coefficient	−40°C ≤ Ta ≤ 85°C		±100		ppm /°C

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C) except Detector Threshold Temperature Coefficient.

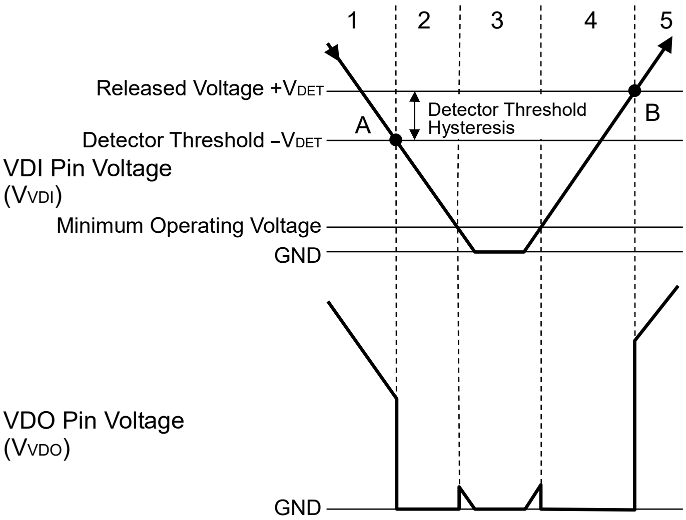
(1) The UVLO detector threshold and the UVLO release voltage are between the min and max of UVLO with Typ. 0.02 V hysteresis.
(2) $-V_{DET}$ is defined as an actual detector threshold and $-V_{SET}$ is defined as a preset detector threshold.
(3) Each minimum value is the value of input voltage when the output voltage is maintained at 0.1 V or less.
(4) Refer to *"Release Output Delay Time"* for details.

OPERATING DESCRIPTIONS

Voltage Detector Section



R5542Zxx2B Block Diagram



Step		1	2	3	4	5
Comparator (-) Pin Input Voltage		I	II	II	II	I
Comparator Output		L	H	Indefinite	H	L
Tr.1		OFF	ON	Indefinite	ON	OFF
Output Tr.	Pch	ON	OFF	Indefinite	OFF	ON
	Nch	OFF	ON	Indefinite	ON	OFF

I $\quad \frac{Rb+Rc}{Ra+Rb+Rc} \times V_{VDI}$

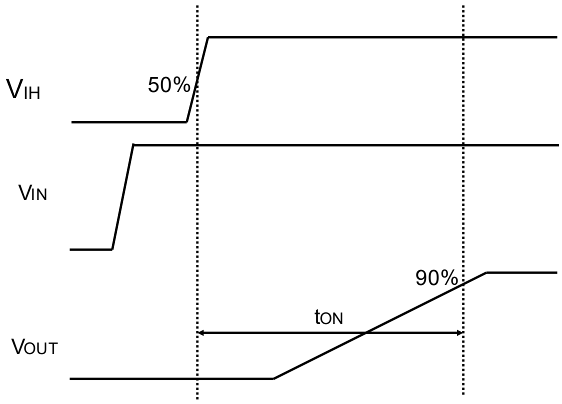
II $\quad \frac{Rb}{Ra+Rb} \times V_{VDI}$

Operation Diagram

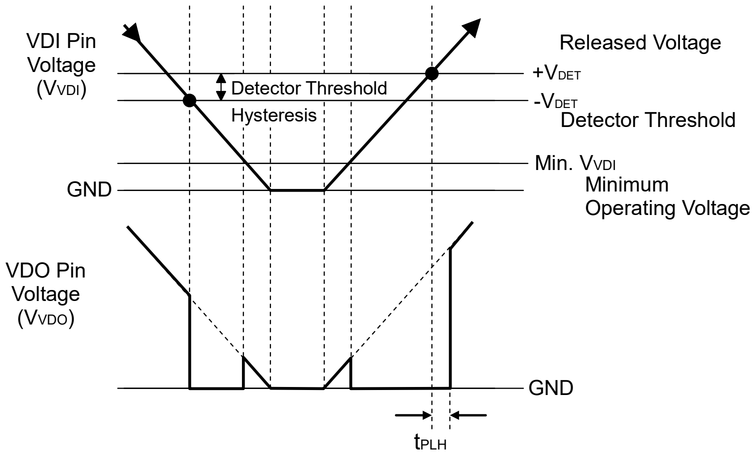
1. The V_{VDO} voltage is equalized to the V_{VDI} voltage.
2. The V_{VDI} voltage drops to the detector threshold (A point) which means Vref ≥ V_{VDI} x (Rb+Rc) / (Ra+Rb+Rc). The comparator output shifts from “L” to “H” voltage and the VDO pin voltage will be equalized to the GND voltage.
3. If the V_{VDI} voltage is lower than the minimum operating voltage, the V_{VDO} voltage becomes unstable.
4. The VDO pin voltage is equalized to the GND voltage.
5. The V_{VDI} voltage becomes higher than the release voltage (B point) which means Vref < V_{VDI} x Rb / (Ra+Rb), and the comparator output shifts from “H” to “L” voltage, and the VDO pin voltage is equalized to the V_{VDI} voltage.

   Note: The difference between a released voltage and a detector threshold voltage is a detector threshold hysteresis.

Timing Chart



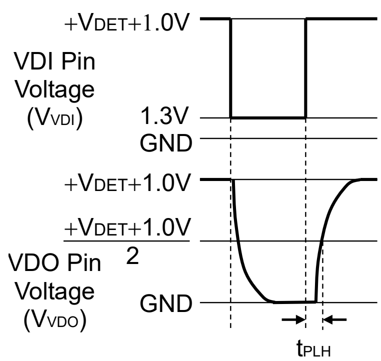
R5542Zxx2B Load Switch Section



R5542Zxx2B Voltage Detector Section

Release Output Delay Time (t_{PLH})

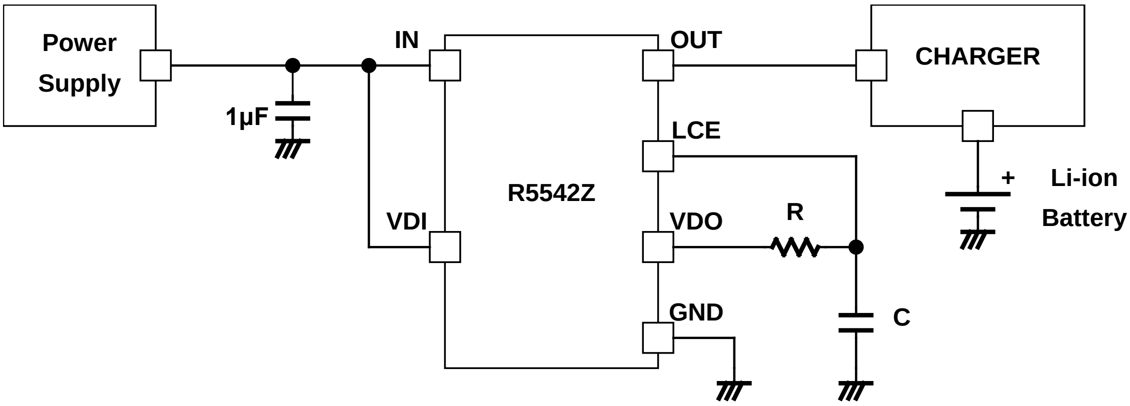
Release output delay time starts when the V_{VDI} voltage is shifted from 1.3V to $+V_{DET}$ + 1.0V and ends when the output voltage reaches ($+V_{DET}$ + 1.0V) / 2.



R5542Zxx2B Release Output Delay Time

APPLICATION INFORMAITON

Typical Application Circuit



R5542Zxx2B Typical Application Circuit

TECHNICAL NOTES

The R5542Z does not require any bypass capacitor between IN and GND. However connecting 1µF or more capacitor between IN and GND may improve the performance against noise. To make delay time from detect input voltage drop to load switch turn off, connect resistor and capacitor between VDO and LCE.

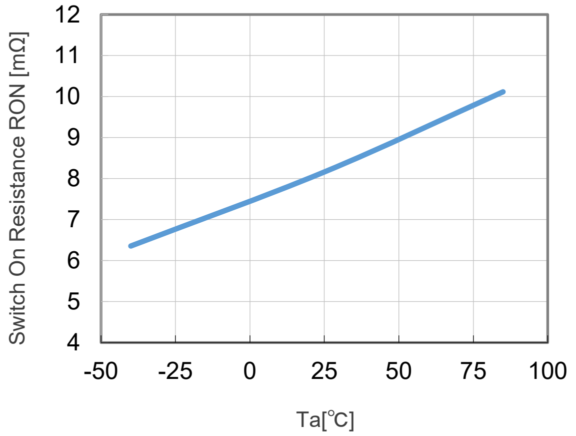
If the ramp rate of "IN" is faster than 50mV/µs, some voltage glitch may appear on "OUT". The glitch level depends on the capacitance connected to "OUT" and the ramp rate of ”IN”.

TYPICAL CHARACTERISTICS

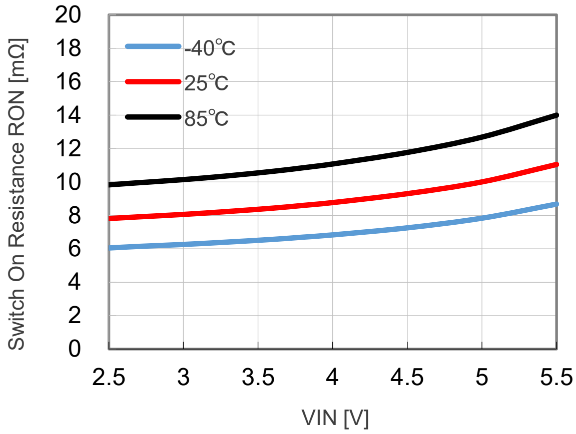
Typical Characteristics are intended to be used as reference data, they are not guaranteed.

1) ON Resistance vs. Temperature / Input Voltage

V_{IN} = 3.0V / I_{OUT} = 500mA

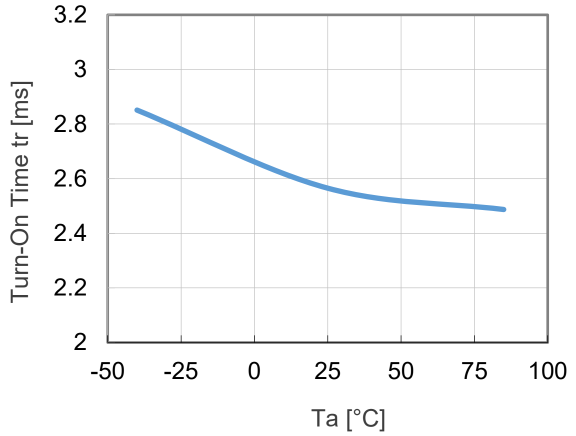


I_{OUT} = 500mA / Ta = 25℃

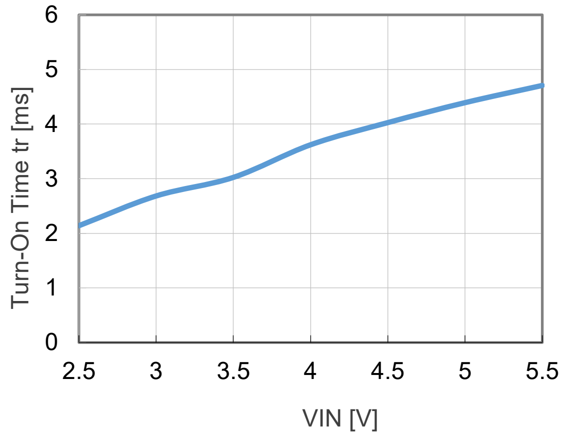


2) Rising Time vs. Temperature / Input Voltage

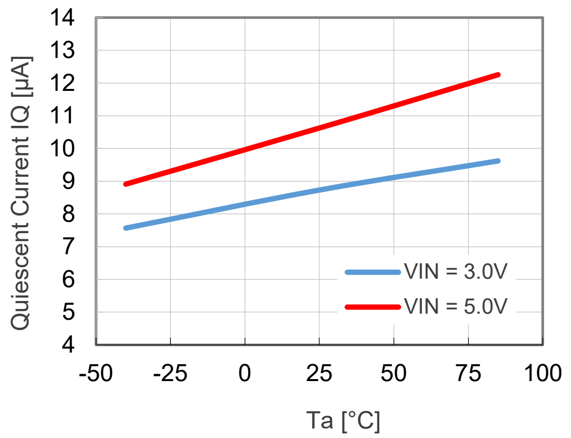
V_{IN} = 3.0V / R_{LOAD} = 50Ω / C_{OUT} = 10μF

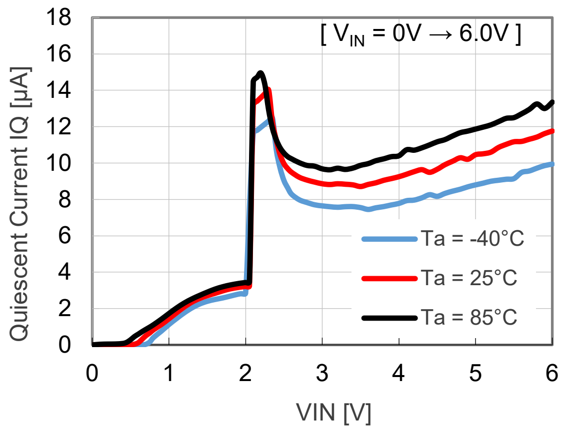


R_{LOAD} = 10Ω / C_{OUT} = none / Ta = 25℃

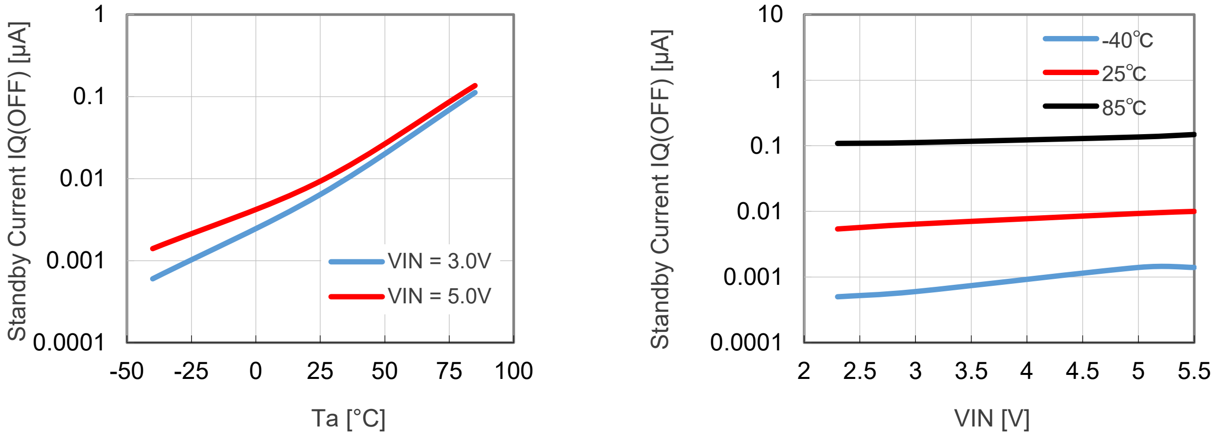


3) SW Supply Current vs. Temperature / Input Voltage

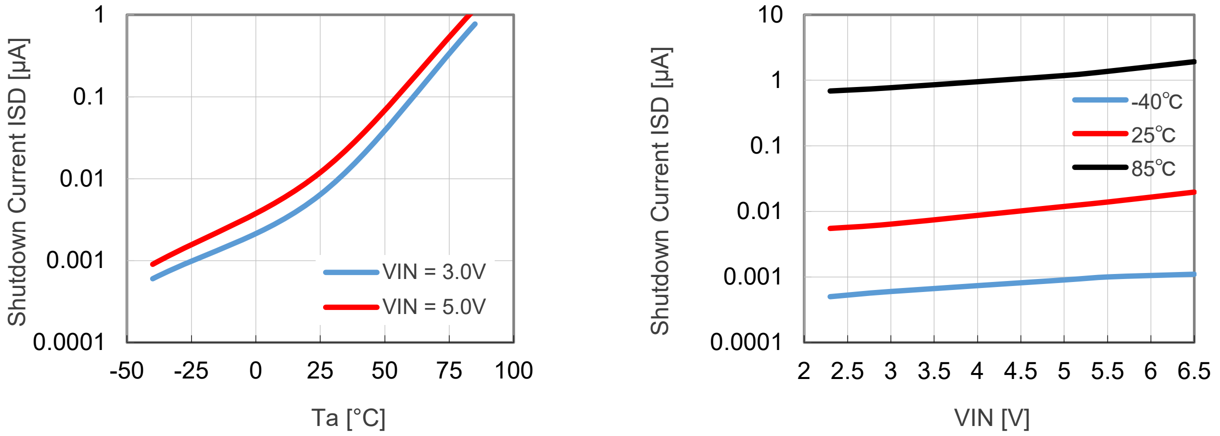




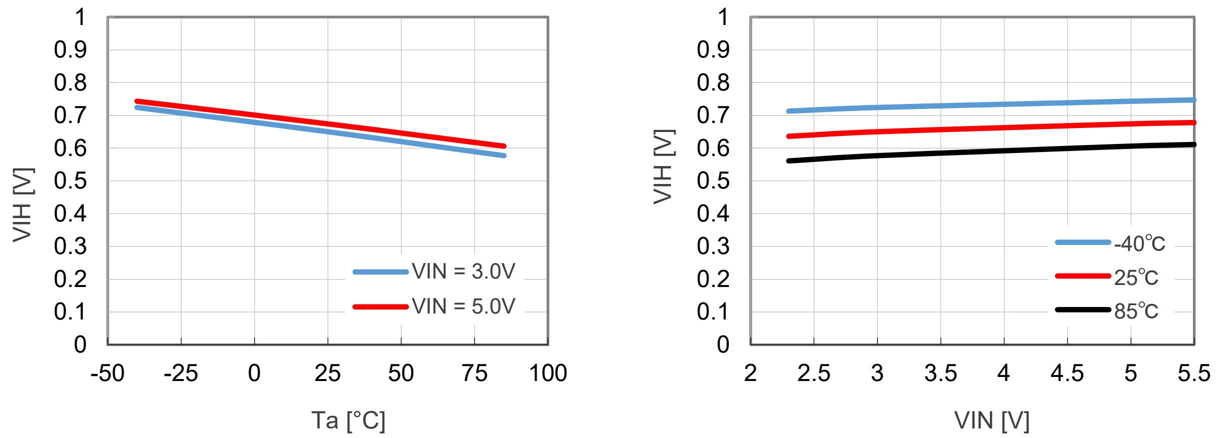
4) SW Standby Current vs. Temperature / Input Voltage



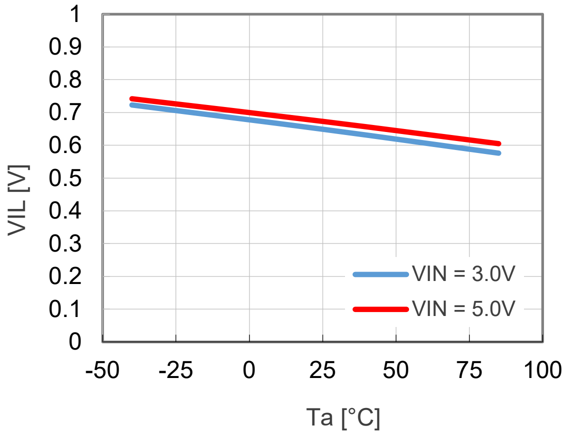
5) SW Shutdown Current vs. Temperature / Input Voltage

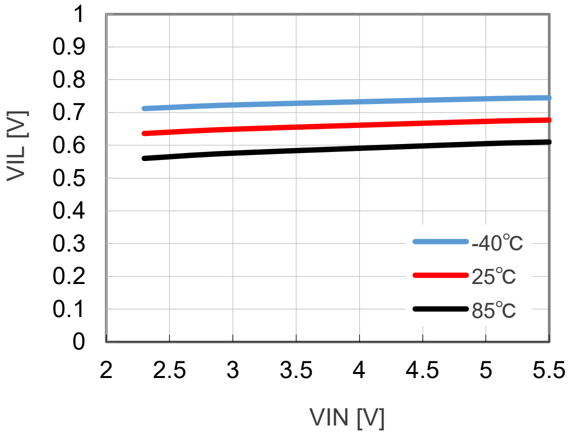


6) V_{IH} vs. Temperature / Input Voltage

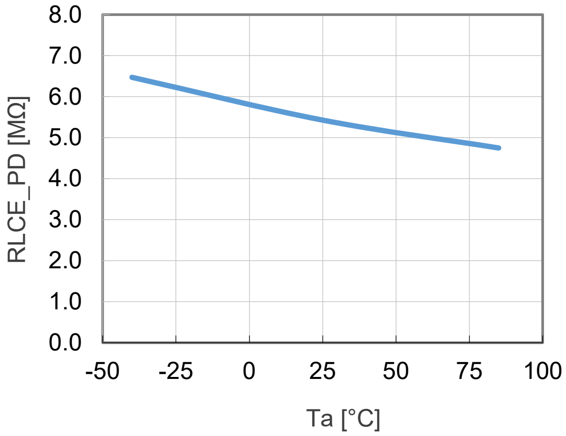


7) V_{IL} vs. Temperature / Input Voltage

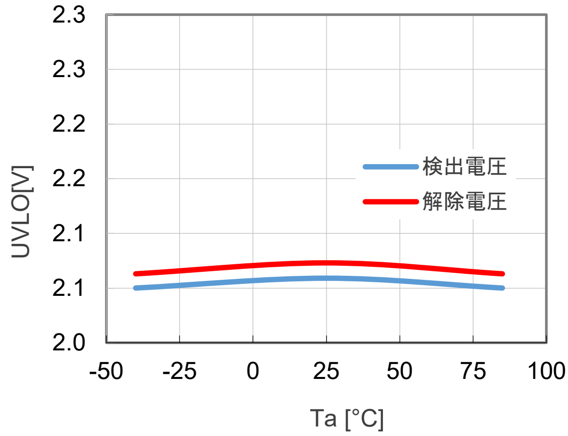




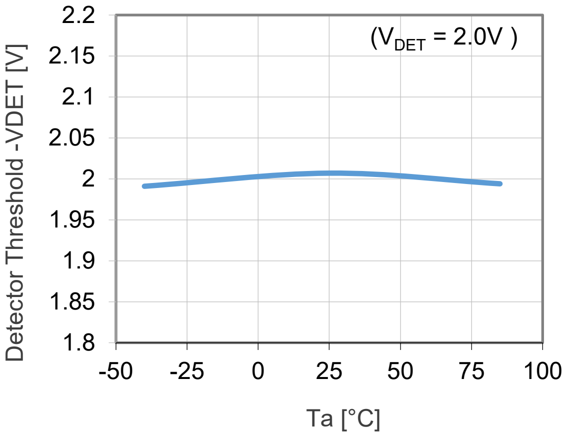
8) LCE Pull-down Resistance vs. Temperature

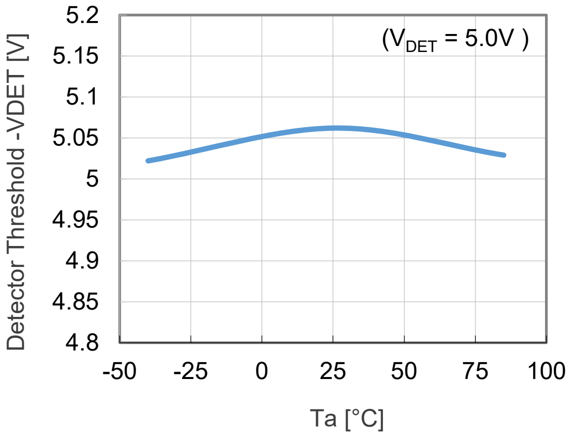


9) UVLO Detection/Release Voltage vs. Temperature

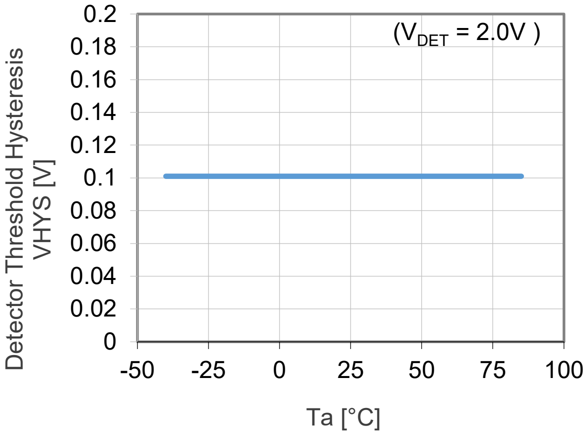


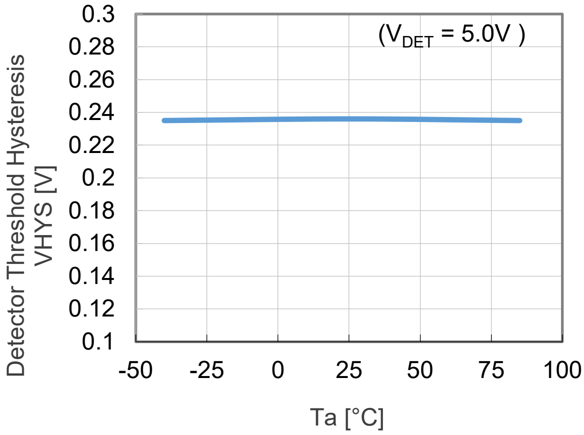
10) VD Detection Voltage vs. Temperature



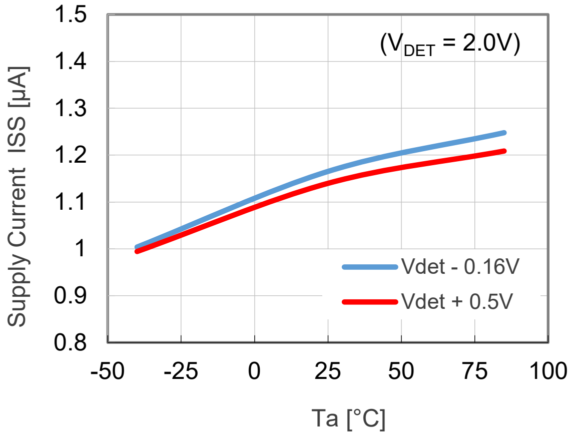


11) V_{HYS} vs. Temperature

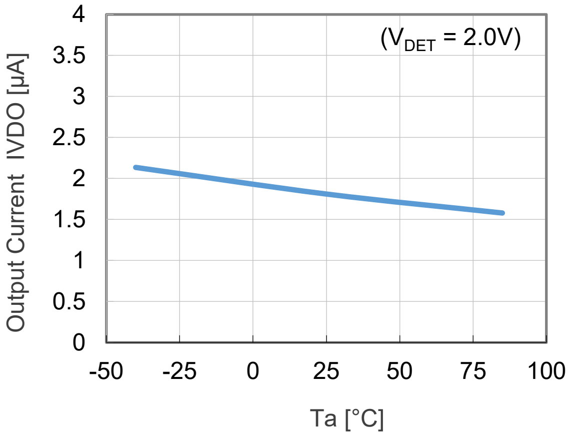




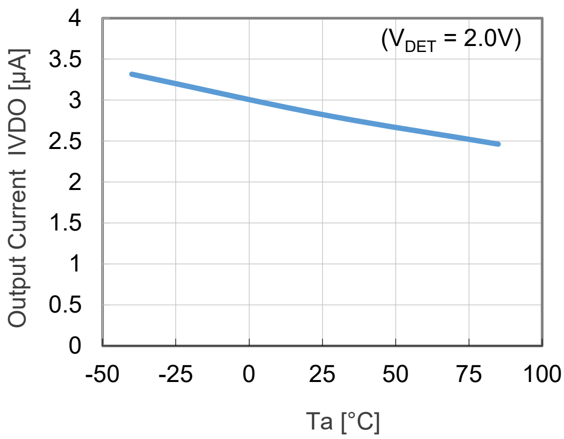
12) VD Supply Current vs. Temperature



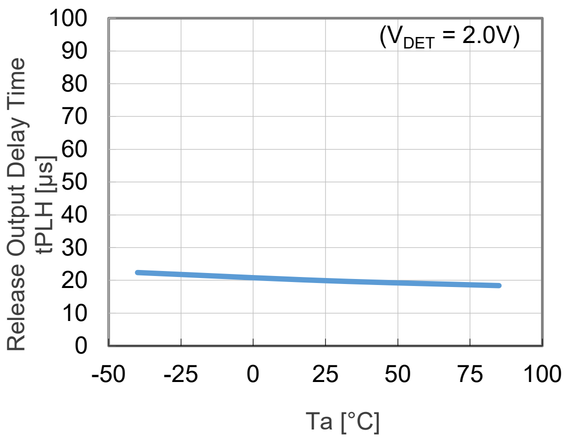
13) Nch Dr. Output Current vs. Temperature



14) Pch Dr. Output Current vs. Temperature

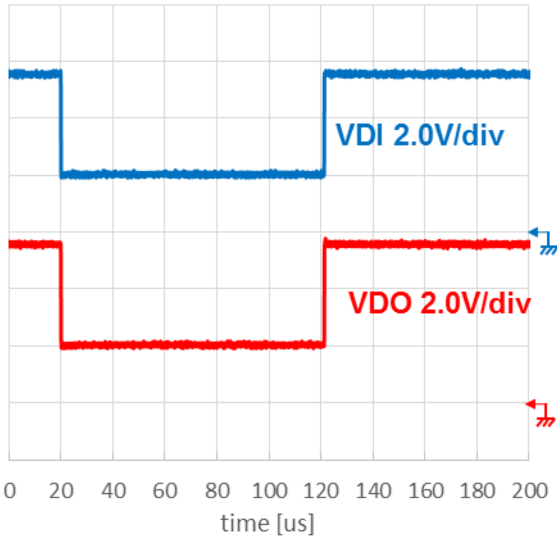


15) Release Output Delay vs. Temperature

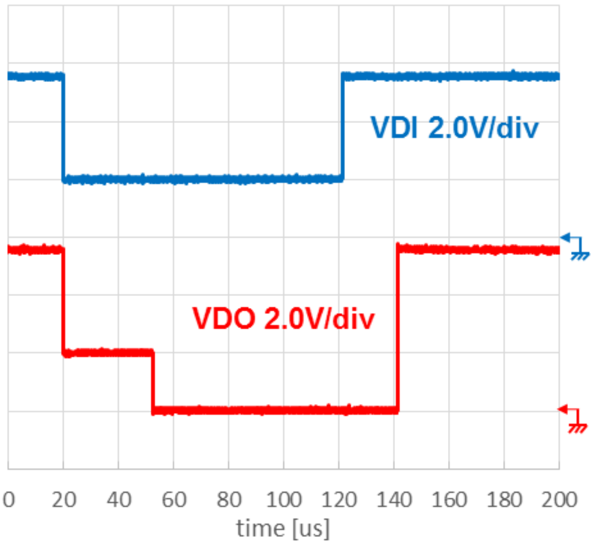


16) VD Transient
Set-V_{DET} = 2.0 V

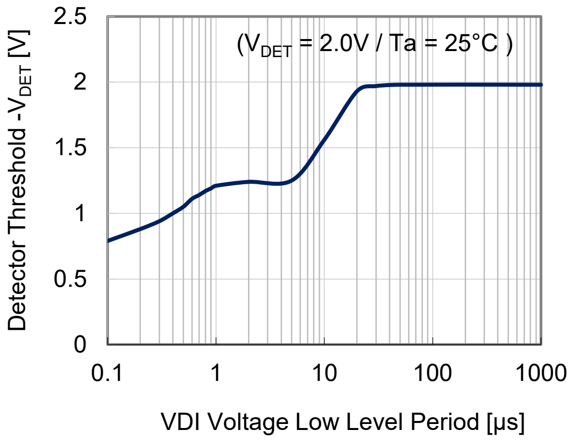
V_{DI} "L" = 2.01 V
5.5V <-> -V_{DET} + 10 mV



V_{DI} "L" = 1.99 V
5.5V <-> -V_{DET} – 10 mV



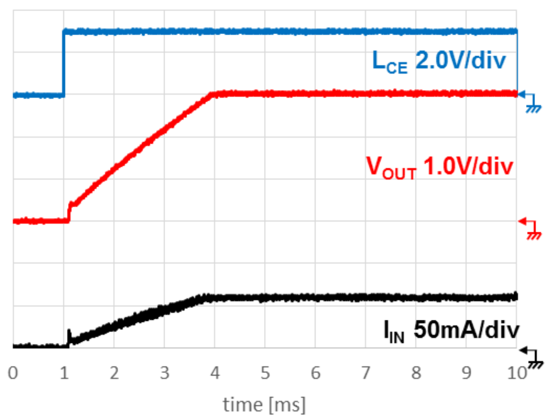
17) VD Glitch



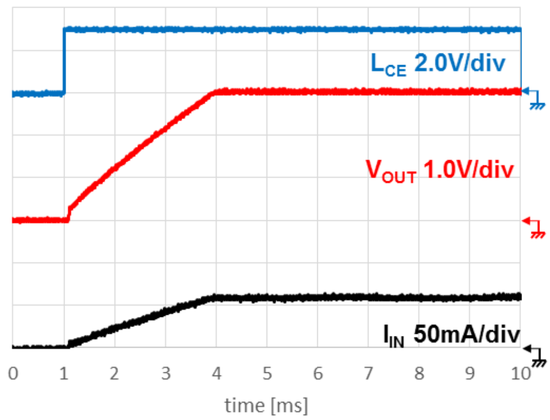
18) SW Inrush Current

V_{IN} = 3.0V / R_{LOAD} = 50Ω

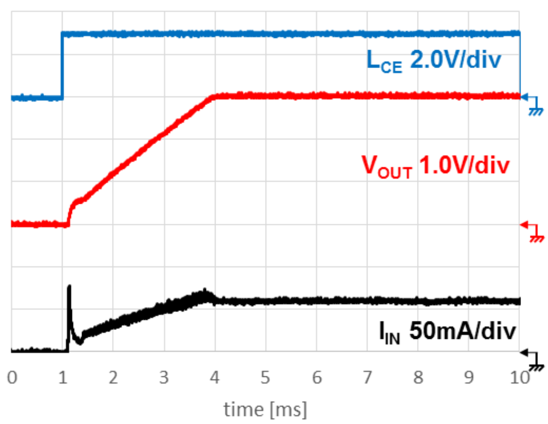
C_{OUT} = 0.1μF



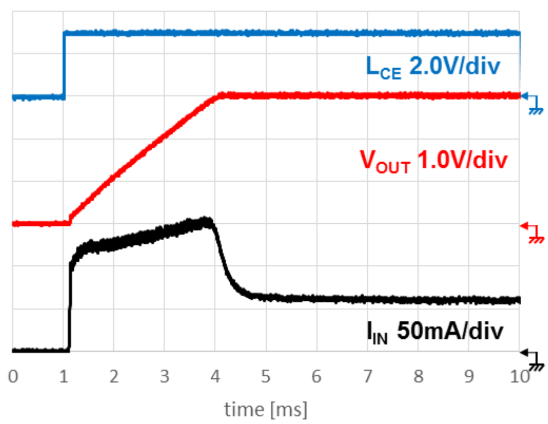
C_{OUT} = 1.0μF



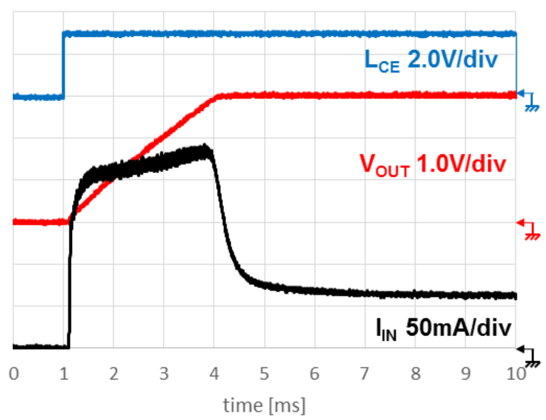
C_{OUT} = 10μF



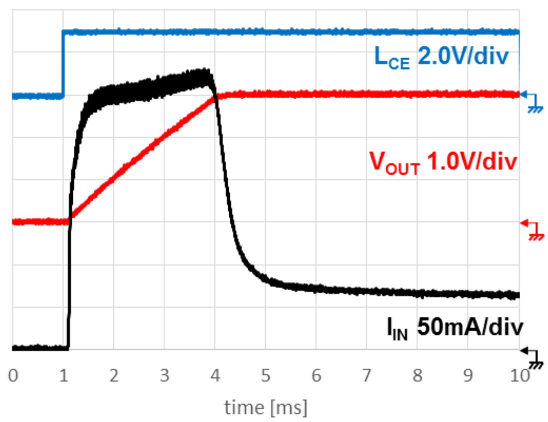
C_{OUT} = 100μF



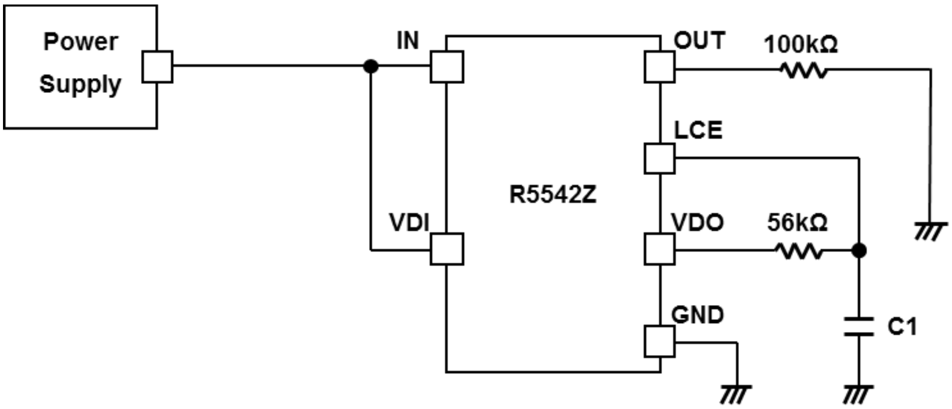
C_{OUT} = 100μF × 2



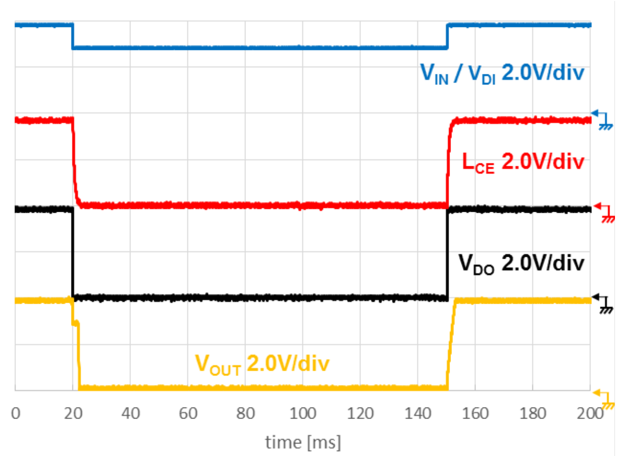
C_{OUT} = 100μF × 3



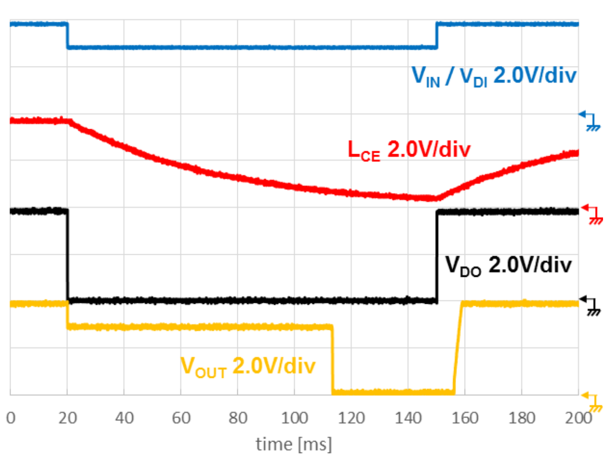
19) VD-SW Reset



V_{IN} = V_{DI} = 3.8V <-> 2.8V / C1 = 0.01μF

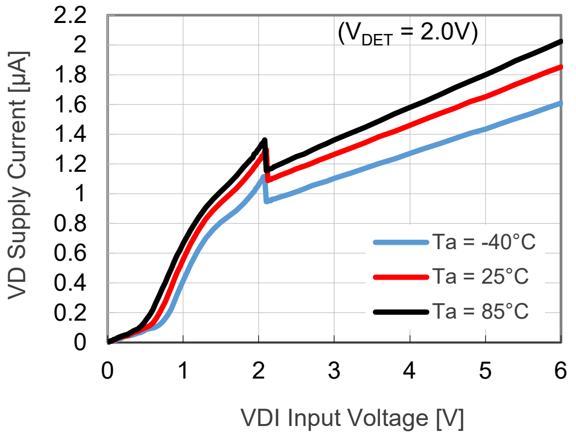


V_{IN} = V_{DI} = 3.8V <-> 2.8V / C1 = 1.0μF

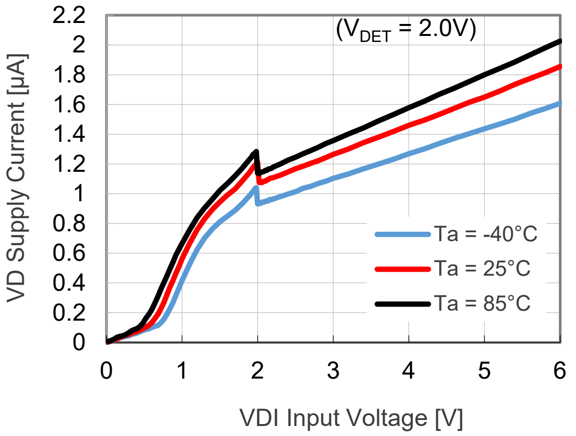


20) VD Supply Current vs. Input Voltage

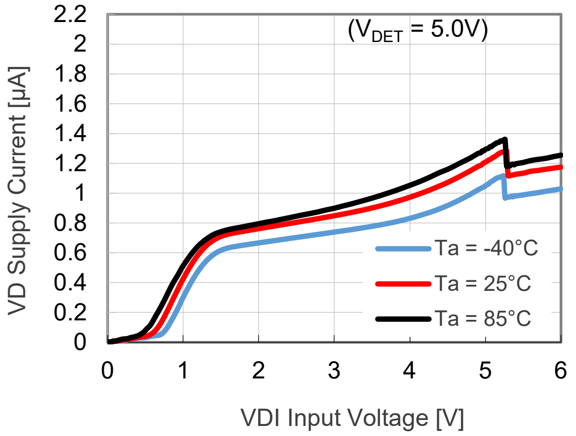
V_{DI} = 0 V → 6.0 V



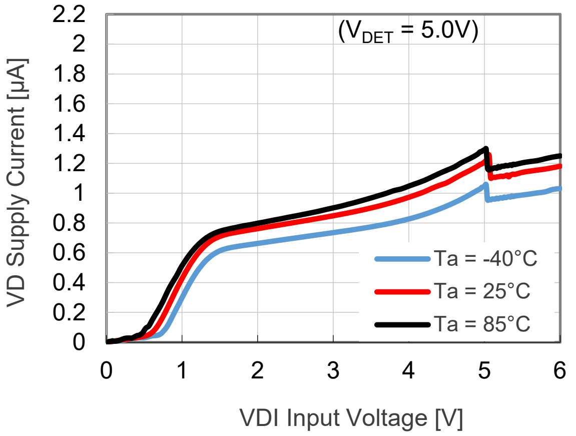
V_{DI} = 6.0 V → 0 V



V_{DI} = 0 V → 6.0 V



V_{DI} = 6.0 V → 0 V



Ver. B

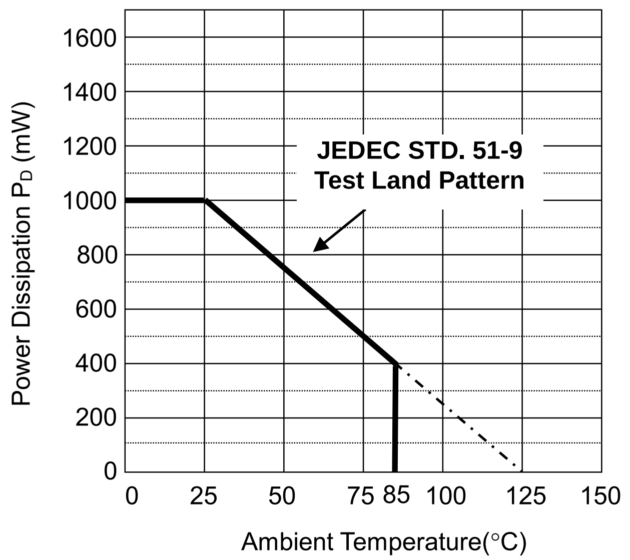
The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement.

Measurement Conditions

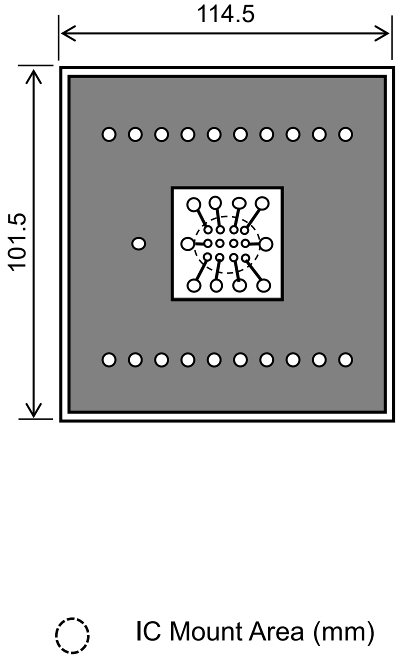
	JEDEC STD. 51-9 Test Land Pattern
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	101.5 mm x 114.5 mm x 1.6 mm
Copper Ratio	Outer Layers (First and Fourth Layers): Approx. 60% Inner Layers (Second and Third Layers): Approx. 100%

Measurement Result (Ta = 25°C, Tjmax = 125°C)

	JEDEC STD. 51-9 Test Land Pattern
Power Dissipation	1000 mW
Thermal Resistance	θja = (125 − 25°C) / 1.0 W = 100 °C/W

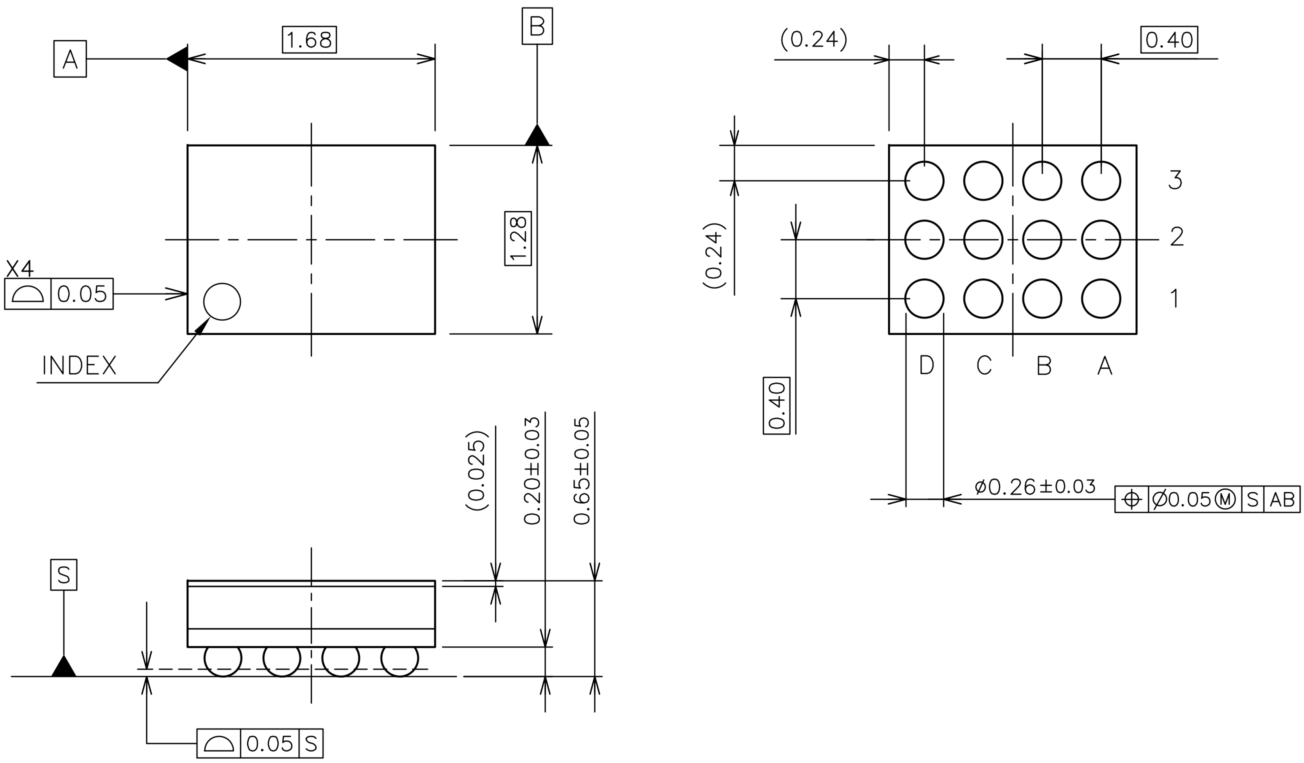


Power Dissipation vs. Ambient Temperature

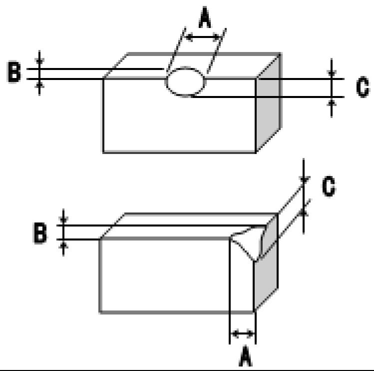


Measurement Board Pattern

Ver. B



WLCSP-12-P3 Package Dimensions (Unit: mm)

No.	Inspection Items	Inspection Criteria	Figure
1	Package chipping	A≥0.2mm is rejected B≥0.2mm is rejected C≥0.2mm is rejected And, Package chipping to Si surface and to bump is rejected.	
2	Si surface chipping	A≥0.2mm is rejected B≥0.2mm is rejected C≥0.2mm is rejected But, even if A≥0.2mm, B≤0.1mm is acceptable.	
3	No bump	No bump is rejected.	
4	Marking miss	To reject incorrect marking, such as another product name marking or another lot No. marking.	
5	No marking	To reject no marking on the package.	
6	Reverse direction of marking	To reject reverse direction of marking character.	
7	Defective marking	To reject unreadable marking. (Microscope: X15/ White LED/ Viewed from vertical direction)	
8	Scratch	To reject unreadable marking character by scratch. (Microscope: X15/ White LED/ Viewed from vertical direction)	
9	Stain and Foreign material	To reject unreadable marking character by stain and foreign material. (Microscope: X15/ White LED/ Viewed from vertical direction)	

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8. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
9. WLCSP products should be used in light shielded environments. The light exposure can influence functions and characteristics of the products under operation or storage.
10. There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or our distributor before attempting to use AOI.
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